






**FPGA Architecture using multiplexers that incorporate a logic gate****Publication number:** JP2001500682 (T)**Publication date:** 2001-01-16**Inventor(s):****Applicant(s):****Classification:**- **international:** H03K19/173; H03K19/177; H03K19/173; H03K19/177; (IPC1-7): H03K19/177- **European:** H03K19/173C2; H03K19/177; H03K19/177B**Application number:** JP19980512626T 19970616**Priority number(s):** WO1997US10279 19970616; US19960708247 19960903**Also published as:**

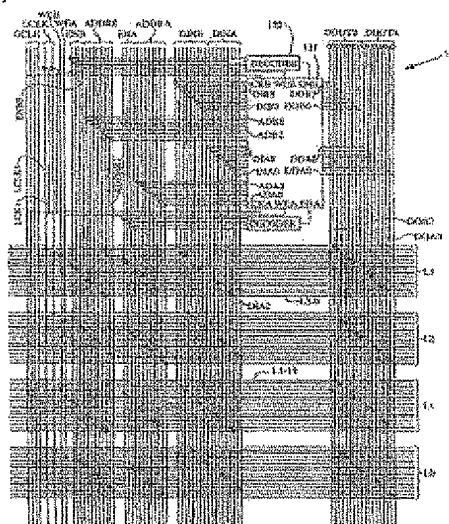
 US6144220 (A)  
 US5933023 (A)  
 WO9810517 (A1)  
 EP0925649 (A1)  
 EP0925649 (B1)

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Abstract not available for JP 2001500682 (T)

Abstract of corresponding document: **US 6144220 (A)**

A structure in which blocks of random access memory, or RAM, are integrated with FPGA configurable logic blocks. Routing lines which access configurable logic blocks also access address, data, and control lines in the RAM blocks. Thus, the logic blocks of the FPGA can use these routing lines to access portions of RAM. According to the invention, a decoder which enables dedicated RAM is configurable to respond in many different ways to decoder input signals. The decoder can be programmed to be enabled by any combination of decoder input signals and can be programmed to ignore any number of decoder input signals. The ability to ignore input signals is important in FPGAs because it saves having to route a disabling signal to an unused decoder input terminal. The decoder can also be programmed to be disabled regardless of decoder input signals. The decoder can be programmed to treat a set of input signals as an address, and can invert or not invert the address.



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